A New Technique to Extract the Gate Bias Dependent S/D Series Resistance of Sub-100nm MOSFETs

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Abstract

In this study, a new technique to extract the S/D series resistance (R_{sd}) from the total resistance versus transconductance gain plot $R_{tot}(1/\beta)$ is proposed. The technique only requires the measurement of $I_d(V_{gs})|_{Vgt}$ and β, allowing fast and statistical analysis in an industrial context. Unlike the usual $R_{tot}(L)$-based techniques, it has the advantage of being insensitive to the channel length and mobility variations and finally enables to extract very accurate values for $R_{sd}(V_{gs})$ and the effective mobility reduction factor $\mu_{eff}(V_{gt})/\mu_{eff}(0)$.

Introduction

The S/D resistance (R_{sd}) is a major concern for the MOSFET scaling as it plays a key role in device performance and power consumption [1]. Since the channel length is scaled down, the R_{sd}/R_{tot} ratio becomes higher and R_{sd} requires improved accuracy in extraction techniques to be assessed within a reasonable error. As described on Fig.1, a transistor can be modeled in linear regime by a channel resistance R_{ch} connected to the S/D series resistance $R_{sd} = R_s + R_d$ through which the drain current I_d flows ($R_{tot} = R_{sd} + R_{ch}$). Due to pockets implants, strain booster and neutral defects, the effective mobility (μ_{eff}) changes as a function of channel length (L_{eff}) [2]-[4] (Fig.2). As a consequence, R_{ch} is no more strictly proportional to the geometrical dimensions of the channel and all $R_{tot}(L)$-based techniques [5-7] fail when $\mu_{eff}(L)$ variations are not properly compensated for [8] (cf. Fig.3). To solve this issue, a new extraction technique based on the relationship between R_{tot} and the transconductance gain β of the transistor in linear regime is proposed. The technique is insensitive to the $\mu_{eff}(L)$, $L_{eff}(L)$ variations (which generally make the other techniques inaccurate) and provides a straightforward way to extract R_{sd} statistically.

The $R_{TOT}(1/\beta)$ technique

The $R_{tot}(1/\beta)$ technique relies on the BSIM3v3 model (1) which reproduces the drain current behavior in linear regime. In (1), $V_{gt} = (V_{gs} - V_{th})$ is the gate overdrive, $\beta=\mu_{eff}(0).C_{ox}.W_{eff}/L_{eff}$ is the transconductance gain (where $\mu_{eff}(0)$ is the effective mobility extrapolated to V_{gt} = 0V) and (Θ_1, Θ_2) are the first and second order mobility attenuation factors, respectively.

$$I_d = \mu_{eff} C_{ox} \frac{W}{L} V_{gt}\left(V_{ds} - R_{sd} I_d\right) = \frac{\beta V_{ds} V_{gt}}{1 + \Theta_1 V_{gt} + \Theta_2 V_{gt}^2} \qquad (1)$$

The channel resistance is defined as $R_{ch} = V_{d,0}/I_{d,0}$ (where the "$_0$" subscript refers to the intrinsic value of the parameter, for R_{sd}=0 Ω.µm). From (1), R_{tot} can be expressed as (2).

$$R_{tot} = \frac{1}{\beta} \cdot \left(\frac{1 + \Theta_{1,0} V_{gt} + \Theta_{2,0} V_{gt}^2}{V_{gt}} \right) + R_{sd}\left(V_{gs}\right) \qquad (2)$$

When V_{gt} is fixed once for a full set of devices with several channel lengths, the $R_{tot} = f(1/\beta)$ plot shows a linear behavior which returns the mobility reduction from the slope (3) and the $R_{sd}|V_{gt}$ from the y-axis intercept (2). By repeating the same extraction for several gate overdrives, $R_{sd}(V_{gs})$ and $\mu_{eff}(V_{gt})/\mu_{eff}(0)$ can be extracted

$$V_{gt} \cdot \left.\frac{\partial R_{tot}}{\partial(1/\beta)}\right|_{V_{gt}} = 1 + \Theta_{1,0} V_{gt} + \Theta_{2,0}.V_{gt}^2 = \frac{\mu_{eff}(0)}{\mu_{eff}(V_{gt})} \qquad (3)$$

Results

The following results were obtained by measurements on our 45nm node technology platform on the low stand-by power devices, featuring 1.7nm-EOT SiON gate dielectric with polysilicon gate and tensile contact etch stop layer for nMOS mobility optimization [9] (Fig.1). Extraction also been performed on FDSOI devices featuring metal gate (WN) with 2.5nm EOT $HfSi_xO_yN_z$ dielectric, 12nm thinned Si film and elevated S/D [10]. Statistical $I_d(V_{gs})$ measurements (72 dices) have been performed for lengths ranging from 35nm to 240nm and W=1µm. Strong pockets implants have been used in the process to increase the channel doping and limit the short channel effect in the smallest devices. V_{th} and β can be extracted from the McLarty's function [11] (4) or from the ξ-function [12] which have both the advantage of being insensitive to (Θ_1, Θ_2) when R_{sd} has a linear variation with V_{gs}.

$$\left(\frac{\partial^2 R_{tot}}{\partial V_{gs}^2} \right)^{-1/3} = \left(\frac{\beta}{2} \right)^{1/3} V_{gt} \qquad (4)$$

Note that, as displayed in the inset of Fig.4, V_{th} deduced from McLarty's functions and ξ-function corresponds to the charge threshold voltage at strong inversion i.e. where $Q_{inv} = C_{ox}.V_{gt}$. $V_{th}(L_{eff})$ and $\beta(L_{eff})$ behavior are displayed on Fig.4 and Fig.5, where L_{eff} has been extracted from C-V measurements [13]. R_{tot} has been measured for each device at several gate overdrive ranging from 0.1 to 1.1V (the nominal voltage for this technology is V_{gs} = 1.1 V, i.e. $V_{gt} \approx 0.4$V). $R_{sd}(V_{gt})$ has been extracted from the R_{tot}=f(1/β) plot, as described previously (2). The linear regression is displayed on Fig.5, where data has been filtered with a recursive normal filter within a ±3σ-tolerance (99% confidence). The points show a very good alignment which results in a very small error on the final result: R^2>0.99, R_{sd} = (110 ± 3) Ω.µm. Fig.7 shows $R_{sd}(V_{gs})$, where V_{gs} has been approximated to $V_{gs} \approx V_{gt} + \langle V_{th}(L)\rangle$, $\langle V_{th}(L)\rangle$ being the average V_{th} for the set of devices: $V_{gs} \approx V_{gt}$ + 0.69 ± 0.05 V (cf. Fig.4). The behavior of $R_{sd}(V_g)$ is consistent with previous studies [14]. Results extracted for small gate overdrive (V_{gt}≤0.2V) show a slight deviation, which might be due to the limited accuracy in the V_{th}-extraction technique and/or non validity of strong inversion approximation close to V_{th}. Intrinsic mobility reduction factors have been extracted from (3) to be compared with the Θ(β) technique [15],[16]. As shown on Fig.8 and Fig.9, both techniques provide very close $\Theta_{1,0}$ values but R_{sd} extracted from Θ(β) shows a larger dispersion mainly induced by uncertainties on the Θ_1 parameter extraction. Finally, error resulting from the $\langle V_{th}(L)\rangle$ approximation has also been quantified (Fig10) and R_{sd} has been estimated for the two extraction techniques. Results for bulk and FDSOI MOSFETs are summarized in Tab.1. As expected, FDSOI devices benefit from a lowered R_{sd} thanks to the elevated epitaxial S/D and an improved accuracy is confirmed for the $R_{tot}(1/\beta)$ technique compared to the Θ(β) one.

Conclusion and Perspectives

This study demonstrates the ability of a new $R_{tot}(1/\beta)$ technique to provide $R_{sd}(V_g)$ and $\mu_{eff}(V_{gt})/\mu_{eff}(0)$ values with an improved accuracy thanks to statistical results. Unlike the $R_{tot}(L)$-based technique, the use of 1/β for the x-axis allows to correct any μ_{eff} or L_{eff} variations. The technique only requires to measure $I_d(V_{gs})|_{Vgt}$ and β on several channel lengths. The results match with the Θ(β) technique which suffers from a larger dispersion and requires full $I_d(V_{gs})$-curves measurements to extract R_{sd}. this technique is fully compatible with fast measurement techniques, offering new perspectives towards R_{sd} monitoring and large scale analysis in industrial environment.

Acknowledgments

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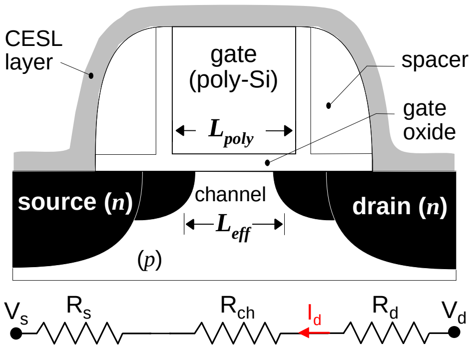

Fig.1 – Typical bulk nMOSFET with tensile contact etch stop layer (CESL).

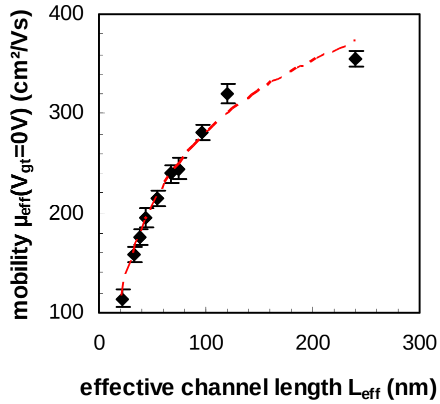

Fig.2 – decrease of the low field mobility for short channel length nMOSFETs

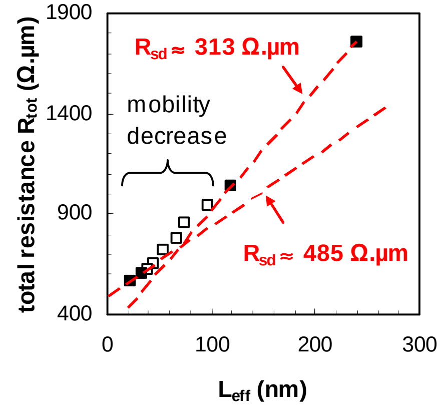

Fig.3 – uncertainty on the $R_{tot}(L)$ technique due to $\mu(L)$ degradation on short channels

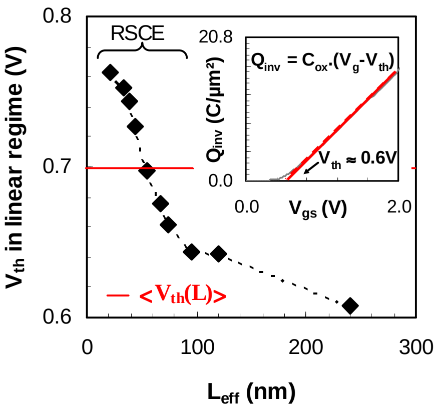

Fig.4 – $V_{th}(L_{eff})$ plot for nMOSFETs in linear regime, in inset: definition of V_{th}.

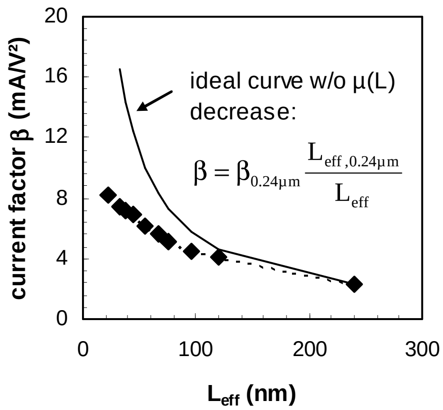

Fig.5 – $\beta(L_{eff})$ measurements. Continuous line: ideal behaviour w/o mobility reduction

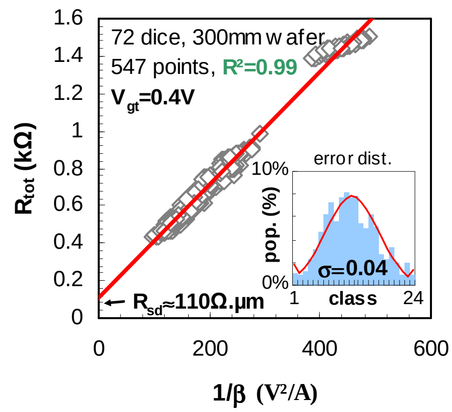

Fig.6 – $R_{tot}(1/\beta)$ plot for nMOSFETs. R_{sd} is extracted from the intercept with the y-axis.

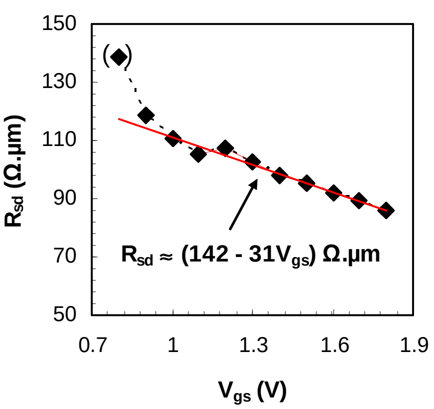

Fig.7 – $R_{sd}(V_g)$ behaviour extracted from the $R_{tot}(1/\beta)$ technique.

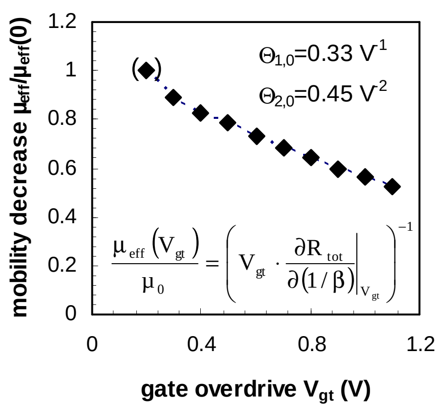

Fig.8 – Mobility decrease (as a function of V_{gs}) from the $R_{tot}(1/\beta)$ technique.

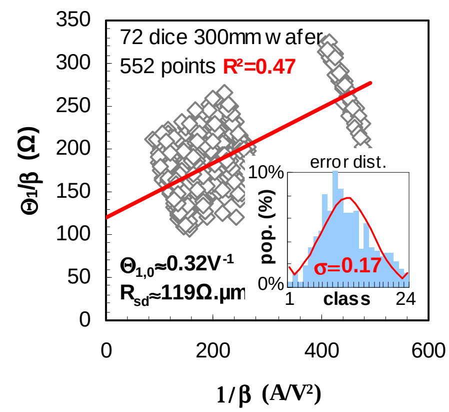

Fig.9 – R_{sd} .and $\Theta_{1,0}$ extracted from the $\Theta_1(\beta)$ technique. In inset: error distribution

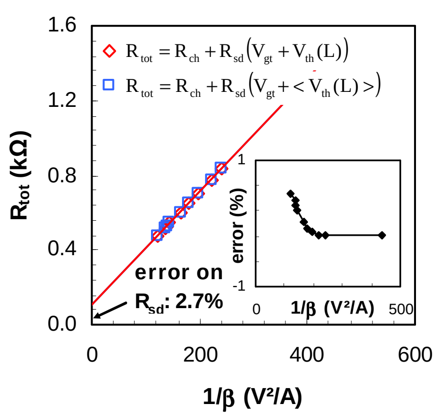

Fig.10 – Comparison between exact model (◇) and approximation (□) using $<V_{th}(L)>$

R_{sd} (Ω.µm)	$R_{tot}(1/\beta)$	Θ(β)
nMOS bulk	110 ± 3	119 ± 10
pMOS bulk	170 ± 5	155 ± 15
nMOS FDSOI	97 ± 5	126 ± 34
pMOS FDSOI	156 ± 5	208 ± 50

Tab.1 –$R_{sd}|V_{gs}$=1.1V values extracted for bulk and FDSOI MOSFETs and compared to results obtained from the Θ(β) technique. As expected, the $R_{tot}(1/\beta)$ method gives more accurate results which remain in line with Θ(β).

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